Guidelines for filling Category-III Proposal

*(The content in **green italics** font is the information that will be needed by the institute while filling the appropriate points in the Category-III Project Proposal. This content could be used as guidelines to assist the institute fill the proposal more effectively.)*

Checklist

Sl. No	Project Details/Supportive Documents	Tick mark (✓)
1.	Part I: Details of Project Proposal	
2.	Part II: Background Information	
3.	Part III: Endorsement from Head of the Institution	
4.	Part IV: Letter of Interest from End User Organization, if any	
5.	Part V: Undertaking from the Chief Investigator of Institution	
6.	AICTE recognized Certificate (Applicable to New Institutions)	
7.	National Board of Accreditation Certificate (Applicable to New Institutions)	
8.	National Assessment and Accreditation Council of UGC (Applicable to New Institutions)	

- *All Institutions falling in the following categories are proposed to be eligible to participate in the programme:*

i. *Indian Institutes of Technologies (IITs)*
ii. *National Institutes of Technologies (NITs)*
iii. *Indian Institutes of Information Technology (IIITs)*
iv. *Indian Institutes of Science Education and Research (IISERs)*
v. *Central Universities/Deemed Universities under Central/State Government*
vi. *Colleges/Institutions of National Importance/Eminence*
vii. *R&D Organizations/Institutions (having B.Tech /MTech/PhD courses)*
viii. *Private Universities/ Private Deemed Universities/Private Colleges ***

*** Private Institutions are also proposed to be eligible for participation in the programme subject to meeting the additional eligibility criteria classified as Clause (A) and Clause (B)*

Clause (A) Criterion for Institutions which have existing M Tech in VLSI / Micro-electronics or equivalent and Cat-III Criteria

- *Institutions that have existing post graduate stream in VLSI / Microelectronics / Electronic Systems / Integrated Circuits / ESDM or equivalent and have produced M Tech / PhDs in these areas for the last 3 years. The PhD student(s) are being admitted as per UGC admission norms.*
- *Institutions should be recognized by AICTE and NBA (National Board of Accreditation) accredited with respect to VLSI / Microelectronics / Electronic System / Integrated Circuits / ESDM or equivalent Programmes.*
  (OR)
- *The Institution should be accredited by NAAC (National Assessment and Accreditation Council of UGC).*

Clause (B) Criteria for Institutions which don't have existing M Tech in VLSI / Micro-electronics or equivalent, but to initiate M Tech programme in VLSI / Micro-electronics or equivalent

- *Institutions should have existing B.E./B.Tech streams in Electrical/Electronics/ Communication Engineering and have produced M.Tech in other areas for the last 3 years.*
- *Institutions should be recognized by AICTE and NBA (National Board of Accreditation) accredited for OTHER specializations (other than VLSI / Microelectronics etc.) M Tech programmes.*
  (OR)
- *The Institution should be accredited by NAAC (National Assessment and Accreditation Council of UGC).*
- *For Cat-III, to encourage the students/researchers from SC/ST/Minority/Women community towards development in VLSI and Embedded System design area, Private SC/ST/Minority and Women University/Institution recognized by government would also be made part of the programme.*

All institutions should furnish copy of documents in support of meeting the above-mentioned eligibility criteria as part of the project proposals.

Based on the above eligibility criteria, it is mandatory to provide the above-mentioned proof/documents for all Institutions. If the mentioned documents are not applicable, provide the justification for the authority/Head of the Institution.

1. *AICTE Certification for MTECH – VLSI / Micro-electronics / Electronic Systems / Integrated Circuits / ESDM or equ.*
2. *NBA Certification for M TECH – VLSI / Micro-electronics / Electronic Systems / Integrated Circuits / ESDM or equ.*
3. *NAAC Certification for the Institution*
4. *If AICTE / NBA / NACC is Not Applicable, Proof document for the establishment of the institution that has been enclosed (Mention the document name and enclose a copy / provide references) and Proof document for the establishment / approval of the COURSES (M.tech VLSI / Micro-electronics / Electronic Systems / Integrated Circuits / ESDM or equivalent) that has been enclosed (Mention the document name and enclose a copy / provide references)*
5. *For Cat-III, proof for the SC/ST/Minority and Women Private University/Institution recognized by government is mandatory.*

Integrate all the supporting documents along with the proposal as single PDF.

Institutions which were part of earlier SMDP-C2SD Category III were involved in development of FPGA based designs. In C2S Programme, it is envisaged/expected that these institutions would preferably submit R&D proposals for ASIC based designs.

The proposals having letter of interest from end-user organizations would be preferred for financial support by MeitY in Category-III.

Note: All Relevant Document to be attached with the Project Proposal

PROFORMA FOR SUBMITTING PROJECT PROPOSAL UNDER CATEGORY III FOR SEEKING FINANCIAL SUPPORT

PART I: DETAILS OF PROJECT PROPOSAL

A. General Information:

1. Title of Project

2. Organization (Nodal Institute)

   a) Name
   b) Address
   c) Legal status (indicate if Government Department, Statutory, Corporate Body, Registered Society, Private Company with recognized R&D unit etc.)

The Institute / Organization has to be clearly identified and mentioned with the details regarding Name, Address and Legal Status etc. (indicate if Government Department, Statutory, Corporate Body, Registered Society, Private Company with recognized R&D unit, Academic Institute (Private / Deemed Univ. / Govt. / Autonomous / Central / State etc.), Autonomous Institution, R&D Organization. etc.)

3. Chief Investigator
   a) Name
   b) Designation
   c) Department
   d) Address
   e) Email ID
   f) Contact No.

The details of CI should be filled here. All the requested details are mandatory to be filled. The CI should have adequate experience of working in VLSI design and related areas.

4. Co-Chief Investigator

   a) Name
   b) Designation
   c) Department
   d) Address
   e) Email ID
   f) Contact No.

The details of Co-CI should be filled here. All the requested details are mandatory. The Co-CI should have adequate experience of working in VLSI design and related areas.

B. Technical Details

1. Aims & Objective of the Project

   The Aims & Objectives of the Project has to be defined clearly and has to bring the details of the outcomes and deliverables more elaborately. Further, the relevance of the technical deliverables to VLSI design and the allied technical domains / topics has to be captured.

2. Novelty/USP of the technology proposed under project proposal

   The proposal needs to capture the novelty and the uniqueness of the proposed technical outcomes / deliverables and how they are of state-of-the art with reference.

3. Detailed description of the Project including block diagram of sub-modules along with their intended functionality.

   The detailed description of the Project including block diagram of each of the sub-modules / units / components along with their intended functionality / utility has to be provided very elaborately.

   For ASIC Design, Fabrication support at SCL will only be provided under category-III.

   ASIC/IP Core related work cannot be outsourced. Only PCB design, assembly, manufacturing, fabrication, packaging etc. can be outsourced.

   If it's an ASIC design and has some on chip components such as sensors, MEMS based design, or any on-chip resistor/capacitor/inductor, any type of device analysis, its requested to do feasibility study and analysis with SCL PDKs and if foundry is feasible, kindly get a letter of confirmation. Kindly note, this is not a mandatory requirement.

   If the work has planned to use VEGA / SHAKTI / AJIT processor as part of SoC, the proposal needs to clearly indicate adoption of any of VEGA / SHAKTI / AJIT processor variant for the project. Or, any other processor is proposed to be adopted for the project needs to be clearly indicated. A broad technical specification of the processor variant (VEGA / SHAKTI / AJIT) or any other processor that has been proposed / chosen has to be captured in the proposal.

   A letter of support from the respective processor team (VEGA / SHAKTI / AJIT / any other processor core) has to be obtained with the following details OR If the respective processor team is part of the project as Nodal / Participating Institute / Startup, the proposal needs to capture the following details:

   a) Variant of the particular processor and the specification of that variant, peripherals, other IPs from the processor team proposed to be provided to this particular project

   b) Licensing Policies and IP rights for the above listed Processor variant

   c) IP rights of the final SoC / enhanced processor cores outcomes etc.

d) Roles and responsibilities of the respective processor team on this proposed project

Kindly contact the Single Point of Contacts (SPOCs) mentioned below for more details / inputs / technical clarifications / licensing policy / IP rights / roles of the processor team etc. on adopting the processor for the project:

- *SPOC for SHAKTI (IIT-M): Vasan V S, Senior Project Advisor, IIT Madras, Mob: 9840872283, email: vasan.vs@gmail.com*
- *SPOC for VEGA (CDAC): Libin TT, Scientist F, CDAC Trivandrum, Mob: 98950 60576 email: vega@cdac.in*
- *SPOC for AJIT (IIT-B): Prof Madhav Desai, IIT-B, email: madhav@ee.iitb.ac.in*

4. IPR filed / IP Core available with the institution in the area of application.

   Any IPR filed / IP cores already available with the Institutions, any other third-party IPs in the area of proposal / application that will be used / adopted for the project need to be mentioned. Furthermore, the IP rights (who owns it) of the existing IP cores that will be used and adopted as part of the proposed project should be mentioned.

5. Initial & targeted Technology Readiness Level (TRL) levels

   This point should explain the following,

   I. What is the initial (current) Technology Readiness Level of the proposed deliverables and outcomes of the project that has been attained by the proposal submitters?

   II. A brief description to capture and justify the indicated initial TRL need to be presented.

   III. What is the targeted Technology Readiness Level (final outcome of the proposed project)?

   IV. Proposed plan to reach the final TRL from the current initial TRL. For Cat-III, the targeted TRL is 4 and above.

   Please refer: https://c2s.gov.in/pdf/TRLDefination.pdf

6. Specifications of System/Subsystem/IP core/Product (as applicable) (datasheet template to be attached with the proposal)

   The Section need to enclose the detailed technical specification and data sheet of the proposed system / each subsystem/ hardware IP / SoC / ASIC / product..

7. Similar activity(ies) / project implemented earlier.

   This section needs to capture a survey of similar / related works that have been done by the proposed project team / collaborators and may indicate how the proposal's aims/ objectives

/ outcomes and deliverables relates to the earlier works by the team. Kindly include appropriate reference of literature.

8. Similar activity(ies) being done elsewhere in the country

   This section needs to capture a survey of similar works that are being done elsewhere in the country and compare and contrast with the proposal's aims/ objectives / outcomes and deliverables. Kindly include appropriate reference of literature.

9. Duration of Project ***(5 Years)***

   The duration of the project for Cat-III is 5 years.(Mandatory).

10. Collaboration/link up to be established/proposed for implementing the project.

    Kindly list the details about the collaborator, nature of collaboration and please capture responsibilities of the collaborator.

11. Roadmap and plan for commercialization

    It is preferred that, the scope and roadmap for commercialization and Transfer of Technology / field trials / deployment / technology adoption plans for the outcomes viz. system / hardware IP core / SoC / ASIC etc. can be envisaged and captured in detail in the proposal. Please mention the design details and documents that will be transferred to the possible technology transfer partner: in terms of design document, circuit schematic, RTL, IC layouts, testing and characterization report of the IC, etc. as part of technology transfer. Kindly provide the tentative plan for testing / characterization / prototyping of the outcomes.

12. Expected outcome in physical terms

    The section need to indicate the outcomes of project whether it is related to ASIC / SoC / system / reusable hardware IPs etc. in physical terms. Further, the proposal needs to capture the list of outcomes and deliverables in physical terms and provide a detailed description of each of the physical outcomes.

13. Year-wise deliverables/Outcomes with specific intermediate milestones (in terms of aims and objectives)

Year	Quarterly Milestones	Timelines	Outcomes
1st			
2nd			
3rd			
4th			
5th			

The Year-wise deliverables / Outcomes with specific intermediate quarterly milestones (in terms of aims and objectives, outcomes and deliverables) have to be captured with the details about the responsible entities / collaborators (if any). The quarterly milestones have to be captured for the respective roles, responsibilities, outcomes and deliverables.

The Year-wise is preferred to cover the following (if applicable),

1. *Design/Modeling of the System/IP*
2. *Development of the System/subsystem/IP of the Proposed work*
3. *Verification of the System/subsystem/IP for its functionality/performance etc.,*
4. *Implementation of the System/subsystem/IP in FPGA*
5. *ASIC Implementation [RTL-GDS II flow]*
6. *Tapeout of the Design. If it is an ASIC design, kindly mention the tentative fabrication plan with SCL 180nm.*
7. *Development of Prototyping Board*
8. *Software/firmware Development for System*
9. *Testing / characterization / prototyping of the outcomes*
10. *Field trials and deployment, commercialization plans of the technical outcomes*

14. Detailed PERT/BAR Chart of the project activity (to be attached as separate sheet)

The quarterly milestones / project plans in the form of PERT / BAR chart have to be enclosed in this section. The PERT / BAR chart needs to capture clearly the activities of participating institutions / collaborator (if any) / End-User (if any) separately and clearly and the inter-links among all the collaborators and stakeholders of the project. Further the PERT/BAR chart needs to include design, Development, Prototyping, Testing and Characterization plans, field trials and deployment plans, commercialization plans etc. in detail.

15. Details of Manpower proposed to be generated/trained (year-wise)

a) Type I Manpower (PhD)
b) Type II (M. Tech in VLSI / Embedded System Design)
c) Type III (M. Tech in Computer / Communication / Electronic System / Equivalent with at least two VLSI courses / minor project in VLSI etc.)
d) Type IV (B. Tech with at least two VLSI Courses / minor project in VLSI)
e) Others (Project staff deployed under the project for implementation)

This Section need to include the manpower generation plan for the duration of the project by the institution in VLSI Design (B Tech & M Tech & PhD). Suggested to add the TYPE details like TYPE-I (Manpower (PhD), TYPE-II (M. Tech in VLSI / Embedded System Design), TYPE-III (M. Tech in Computer / Communication / Electronic System / Equivalent with at least two VLSI courses / minor project in VLSI etc.), TYPE-IV (B. Tech with at least two VLSI Courses / minor project in VLSI, Others (project staffs that will be deployed by the

institute for VLSI Design academic activities). Further, the total number of students enrolled / to be enrolled should also be indicated (academic year wise, for all types of manpower).

Number of Manpower proposed to generated/train is to be given considering all students enrolled/to be enrolled in the class (Academic Year-wise)

It can be capture in the table as follows,

Type of Manpower	Year-I	Year-II	Year-III	Year-IV	Year-V
Type I (PhD)					
Type II (M. Tech in VLSI / Embedded System Design)					
Type III (M. Tech in Computer / Communication / Electronic System / Equivalent with at least two VLSI courses / minor project in VLSI etc.)					
Type IV (B. Tech with at least two VLSI Courses / minor project in VLSI)					
Others (Project staff deployed under the project for implementation)					
Total					

Also If the institution is currently NOT offering ME / M Tech in VLSI Design or equivalent, capture the plans including the time schedule have to be included in the proposal to start ME / M Tech in VLSI Design or equivalent.

Institutions should initiate M.Tech in VLSI/embedded system, if not already done within 2-3 years of the initiation of the programme. A declaration is to be provided by the Institution (who do not offer M.Tech course at present) for initiation of M.Tech Program in VLSI/Embedded System in the first 2-3 years of the program with approval of their competent authorities.

16. Outcome in terms of Intellectual Property/Patent

Capture the technical outcomes of the Proposed project that could result in terms of Intellectual Property Rights (could be filed) or Patentable outcomes (probably a list) have to be deliberated (typical idea / novelty) in detail.

C. End User Organization (Letter of Interest to be attached, if any)

a) Details of (likely) application.

R&D project proposals having letter of interest from end user organization would be preferred for support under Category III.

The likely end use applications of all the outcomes of the project is preferred to be captured in detail. Further, how the end user will adopt the outcomes of the project is preferred in detail.

b) Details of (likely) end user organization/ expression of interest received from the end user organization.

It is preferred that the end user organization details have to be captured with information on Name, Address, Legal Status of the End User (as startup / MSME / Industry / Pvt. Company / Public Company / Govt. Dept. or Ministry / Govt. R&D Organization / Private with Recognized R&D Centre or any other kind), etc. Further, indicate whether the LoI with all the details as per the format given in the proposal template has been enclosed as Part – IV.

D. Details of Infrastructure and other facilities available at the participating institute for undertaking the project.

It is mandatory for Institution to make available basic infrastructure such as VLSI Lab, Workstations/Servers (in working condition), lab staff etc. during the entire project duration. No separate hardware platforms like workstations, servers, laptops, etc. would be provided under the project.

a) Lab Infrastructure (Lab space, number of Workstations/Servers etc with specification).
Capture separately the VLSI Lab infra. details viz. lab space, workstations / servers / desktops etc.

b) List of Capital equipment along with model numbers, specifications etc.
Capture the List of Capital Equipment in the VLSI Lab with Model Number, Purpose of Use, Specification in a table.

c) Existing manpower and other personnel with names available for the project on full-time basis.
Capture the Existing manpower and other personnel with names, designation available for the project on full-time basis.

d) Expensive Equipment /facilities available elsewhere which could be made use of for the project.
Capture the Expensive/facilities identified elsewhere which could be made use of for the project. Preferably with the Model Number and details.

E. Details of short term VLSI Design projects for B.Tech/M.Tech/PhD students with plan of execution & timelines.

This section need to mandatorily include the details of 20-25 short-term VLSI Design projects to be undertaken separately by the Institute / Organization for B.Tech / M.Tech / PhD students with plans for execution & timelines for the short term projects. The details need to be captured as per Table presented. The proposed list of short-term projects are as future plans to be done during the proposed project and should not indicate the past projects that have been carried out and completed already. It is preferred that the student tapeouts by the institutions to SCL will be based on these projects. These short-term VLSI project also may include activities apart from the R&D Proposal activities.
Request to capture in the below table

Sl. No.	Project title	Category of Student (B.Tech/M.Tech/ PhD)	Plans for execution	Timelines (Year wise)

F. Financial details:

1. Total Budget outlay

Budget Head	Year Wise Budget Requirement (Rs. In lakh)					
	1st Year	2nd Year	3rd Year	4th Year	5th Year	Total
Capital Equipment (FE Comp)						
Consumable stores. (FE Comp)						
Duty on import (if any)						
Manpower						
Travel & Training (FE Comp)						
Contingencies						
Overheads, if any (Maximum 1% of total Outlay excluding Capital Equipment Budget)						
Grand Total (FE Comp.)						

The financial details / budget requirements for the institute / Orgn. has to be provided year wise with appropriate head wise separately in the table as per the proposal format only. Request not to modify the template. Check whether any errors in summation, incorrect data entry etc. Kindly check the yearly sum and cumulative budget etc. The budget need not be in two / three digits accuracy (post decimal mark) and can be with single digit (at most) fraction or could be as integer without any fraction. The overheads should not be more than 1% of Consumables + Travel and Training + Manpower + Contingencies Budget.
Mention the Total Cost of the Project below the Table in Lakhs.

Institutions to restrict the proposal within the budget outlay of category-III i.e., 86Lakhs in which proposal is being submitted.
No consultancy expenses will be provided under the project and hence the budget table shall not include any kind of consultancy budget head and none of other budget heads can be earmarked for consultancy expenses for CI / Co-CI / Domain Experts / Other Investigators etc.
No separate funds would be provided for creation of new facilities under the programme. However, the Institutions may outsource the project activities like - PCB design, assembly, manufacturing, fabrication, packaging etc. within the approved outlay of the project, which

cannot be undertaken at the Institution. However, no R&D & ASIC/IP Core related work activity under the project can be outsources by the institutions.

2. Capital Equipment Requirement ***(to be provided by all participating Institutions)***

S. No	Name of Capital Equipment	Number	Cost (Rs. in Lakhs)	Justification
1.				
2.				
3.				
4.				

Fill the details of the Capital Equipment Requirement in the above Table.

The Capital Equipment Shall not include the items required for basic infra. such as VLSI Lab establishment, servers, workstations, laptop, Printer, lab staff expenses, buildings (civil infra.) etc. for the Institute / Organization. Financial provisions are NOT SUPPORTED for the above-mentioned items as part of the project and hence the proposal SHALL NOT include the same in the budget for Capital.
Workstations/Servers for 8 North eastern NITs (Rs. 25 lakh/per institute). Separate provision of Capital Equipment for NE Institutions has been kept for upgradation of the VLSI lab facility.

Further, Generic FPGA Boards (Basys3, Boolean, PYNQ, Zedboard, Genesys2 etc.) will be provided as resource to the Participating Institutions of C2S Programme and hence should not be included as part of Capital Equipment List and budget also. Besides, the CE list and budget should not include generic Cadence / Mentor / Synopsys / Xilinx Vivado tools as these tools will also be provided as resources from centralized facility. The Capital Equipment budget is meant for any specialized equipment / Specialized EDA tools/ Specialized High end FPGA Boards (UltraScale/UltraScale+ boards, RFSoC, Alveo etc.), that are required for executing the project to achieve the deliverables and outcomes.

<Preferred FPGA Boards as resource to the institutions in a table>

Request to Capture the generic Cadence / Mentor / Synopsys / Xilinx Vivado tools requirements in the table provided. The EDA tools (Synopsys, Cadence Mentor Xilinx Vivado Only) requirement (typical and tentative) from Centralized Licenses Facility for VLSI Design Projects (STUDENT / ACADEMICS) in Institute have to be captured separately in an indicating name of the vendor (Cadence, Synopsys, Mentor Xilinx Vivado Only), names of the tools and number of licenses (peak and monthly average).

EDA Tool Vendor	Names of the Tool Bundle/tools – List	No. of Licences	
		Peak	Monthly Average
Mentor			

Cadence			
Synopsys			
Xilinx Vivado			

3. Manpower Requirement (Year-wise) with justification *(to be provided by all participating Institutions)*

The manpower Requirements for executing the R&D part of the project has to be captured and the salaries have to be indicated whether it's as per DST norms. Further, manpower meant for RESEARCH only is permitted and administrative staffs are not permitted. A justification note for the required manpower indicating the activities that will be carried out by them have to be included below the Manpower Requirements Table. Request not to modify the template. Fill the entire duration of the project.

S. No	Designation	Monthly Salary	1st Year		… 5th Year		Total
			No. of Posts	Total Expenditure	No. of posts	Total Expenditure	
1							
2							

G. Other information, if any

(To be signed by Institution)

Signature of Chief Investigator
Designation
Date

Signature of Head of the Institution
Designation
Date

PART II: BACKGROUND INFORMATION

1. Title of Project

Mention the title of the Project as same as of the tile mentioned in the Part-I.

2. (i) Chief Investigator
   (ii) Co-Chief Investigator

Kindly add the names of <CI, Co-CI> of Institute / Orgn as same as of Part-I

3. Other Investigators of the Project with their designations

Kindly add the names of TWO MORE faculties / investigators of Nodal Institute / Orgn. and the details. It is expected that they have expertise in VLSI domain related areas.

4. Brief Bio-data of Chief -Investigator and other Investigators (including publications/patents) (Please attach separate sheets)

Kindly add the CVs of CI, Co-CI and two more faculties / investigators of Institute / Orgn. Online links for CVs are not accepted.

5. Competence of Investigator in Project Area (Including Industry interaction/Technology transfer)

The Chief Investigator &/ Co-CI &/ Other 2 investigators / faculties (Institute / Orgn.) of the Proposal should have relevant exposure to VLSI Design / Electronics or allied topics. Support details are to be captured broadly.

6. Other Commitments of the Chief Investigator and Co-Investigators (including lectures, research projects responsibilities etc.) Indicate the percentage of time the Chief Investigator and Co-Investigator would devote to the project.

This section should provide the Other Commitments of the Chief Investigator and Co-Investigators (including lectures, research projects responsibilities etc.)
Also Indicate the percentage of time the Chief Investigator and Co-Investigator would devote to this project.

7. Details on each of the ongoing/completed projects with the Chief Investigator/Co-Chief Investigator/R&D Team

   a) Project Title
   b) Funding Agency (or Internal funding)
   c) Brief Project Summary
   d) Technical Status vis-a-vis objectives
   e) Financial Status (Total Project outlay, expenditure to date)
   f) Duration and year of initiation
   g) Expected date of completion

8. Details of work already done by present investigators/R&D team in this or other areas

   a) Successfully completed on schedule
   b) Currently in progress
   c) Abandoned
   d) Industry interaction/know-how transferred

9. Brief summary of other project proposals (submitted by any of the Investigators) awaiting consideration of MeitY and other funding agencies like DST, DRDO, DSIR, MHRD, ICICI, IDBI etc.

10. List the personnel already working in the organization who would be transferred to work full time on this project.

11. Name of experts whom the Chief Investigator would invite to join the project team as full time/part time member.

PART III: ENDORSEMENT FROM HEAD OF INSTITUTION

(On the Official letter-head)

Project Title: *<Title>*

Project Cost: *<Total Cost as per the Budget table>* **Duration:** *<Project Duration>*

Endorsement by the Head of the Institution

1. I have read the terms & conditions (Annexure -1) (including special terms & conditions for co-financing) governing the grant-in-aid and I agree to abide by them.

2. I certify that I have no objection to the submission of this research proposal for consideration by the Ministry of Information Technology

3. In case the project is approved, I undertake to make available facilities to carry it out, to arrange for the submission of periodic progress reports and other information that may be required by the Ministry of Information Technology and in general to ensure that the conditions attached to the award of such grant are fulfilled by my institution/organization.

4. I certify that in case present chief investigator is not available for any reason to continue work on this project, the following persons will be available to carry it throughout to completion:

S.No.	Name	Designation
1.		
2.		

<It is mandatory to fill the name of the two faculties who is responsible for this project if chief investigator is not available >

5. I certify that the facilities mentioned in the body of this report are available at my institution.

6. I certify that I shall ensure that accounts will be ept of the funds received and spent and made available on demand, as specified and required by the Ministry of Information Technology.

7. I certify that I am the competent authority, the virtue of the administrative and financial powers vested in me by to undertake the above stated commitments on behalf of my institution.

It is mandatory to fill the same content in the Institution letter head and place the seal of the institution along with Signature of the Head of the Institution along with the date.

Signature of the
Head of the Institution
Designation
Date:

PART IV
LETTER OF INTEREST FROM END USER ORGANIZATION (IF ANY)
(On the Official letter-head)

1. Project Title:

2. Duration:

3. Name of End User Organization

4. Brief Business/Organization Profile

5. Roles & Responsibility defined under the Project

6. I have gone through the Project Proposal submitted by ……. (Name of CI of Nodal Institute) of ……..(Name of Nodal Institute) for MeitY funding and noted the obligations and terms and conditions. I understand the responsibilities indicated in our name as stated below:

7. I hereby affirm that my Organization/Industry is committed to participate in the Project to the full extent as indicated in the Project Proposal. A summary profile of my organization is given below:

   <Request to fill the summary profile of the organization - capture the status of the organization, Domain of work etc., Kindly mention detailed specifications, roles and responsibilities, technical contributions, or any kind of support from the organization. Request to capture how the organization is planning to adopt/ use/ deploy the deliverables of the proposal.>

(Head of the End User Organization)
Seal/Stamp

Date:

Place:

PART V
UNDER TAKING FROM THE CHIEF INVESTIGATOR OF THE INSTITUTION

1. I have carefully read the Guidelines, Eligibility Criteria of C2S project available at C2S website and Terms and Conditions of MeitY (Annexure-1) and I agree to abide by them.

2. I have not submitted this or a similar Project Proposal elsewhere for financial support.

3. I shall ensure that accounts will be kept of the funds received and spent and made available on demand, as specified and required by the Ministry of Electronics and Information Technology.

4. I undertake that idle capacity of the permanent equipment procured under the Project will be made available to other users.

5. I have enclosed the following:

   a. Endorsement from the Head of the Institution

   b. Letter of Interest from the End User Organization (if, any)

Chief Investigator (CI):

Name
Signature:
Date:
Place

Co-Chief Investigator (Co-CI):

Name
Signature:
Date:
Place

<Request both CI and Co-CI to duly sign the Undertaking with Date >